A Versatile Receiver IC Supporting WCDMA, CDMA and AMPS Cellular Handset Applications

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***Abstract* — This paper presents a single chip, superhetrodyne receiver IC capable of supporting dual-band, tri-mode handsets. Supported standards include W-CDMA, CDMA (IS-98-C) and AMPS. The receiver consists of multi-step gain LNAs, high performance RF mixers with adjustable linearity, a variable gain amplifier, on chip VCO cores, and an IQ downconverter. The IC is fabricated in a 35GHz f_τ Silicon BiCMOS process [1] and packaged into a 48 pin 7mm x 7mm land grid array (RF-LGA™) chipscale package.**

I. Introduction

In the current wireless handset market, service providers are forced to compete for customers at many different levels. Marketability is enhanced through features such as low cost, small size, long standby and talk times, and multi-band/multi-mode functionality. In response to market's needs, cellular phone manufacturers are increasingly seeking highly integrated radio solutions to provide these features. Further, the integrated radio must be versatile enough to adapt to the different needs of the handset manufacturers.

An integrated solution offers lower total parts count and reproducible performance, which together drive a lower manufacturing cost. Smaller form factors are achieved due to the decreased number of external components, as well as a reduction in total package area. The receiver, shown in Figure 1, consists of low-noise amplifiers in the cellular and PCS bands, two cellular band mixers and one PCS mixer, a variable gain amplifier (VGA) with three inputs, in-phase and quadrature (IQ) demodulators, and two voltage-controlled oscillators (VCOs) for IQ local oscillator (LO) generation. This design provides integration of components needed to achieve radio frequency (RF) to IQ base band downconversion in a superheterodyne architecture.

II. Receiver System Specifications

This receiver was designed to meet the system specifications for AMPS, CDMA, CDMA-PCS, and WCDMA [2,3]. The system specifications for these standards require a high performance radio with a low noise figure (NF), high gain (G), and high input third-order intercept point (IIP3). This highly integrated solution dynamically adapts to the system requirements across the dynamic range of the received signal strength.

As the received signal strength at the antenna of the handset increases, the current consumption of the RF front-end can be reduced due to the lower required gain and reduced NF constraints. For a given signal level, as the blocker levels reduce, the current consumption can be continuously decreased. This is particularly important in a CDMA system, where high gain, high linearity and low noise are required simultaneously at sensitivity.

III. Detailed Circuit Design

A. Low Noise Amplifiers

The CDMA IS-98-C specification tests IIP3 at three signal levels, with the required IIP3 increasing with input signal level. This allows a switched gain LNA with three gain steps, selected by two control pins, to be used in the cellular band. With the increased signal level at each gain step, the system gain required is lower and NF allowed is higher. The required IIP3 can then be achieved using less current.

The major design challenge for the three-step cellular LNA is achieving low NF, high IIP3 and high gain simultaneously to meet sensitivity requirements at the highest gain setting. A common emitter configuration is used to obtain the lowest possible noise figure. Using a large device reduces base resistance (r_b) thermal noise and lowers the contribution of base current shot noise flowing through r_b. The size of the device is limited by the reduction in gain brought on by feedback through the collector base capacitance (C_{CB}) as the device size increases. This reduction in gain eventually causes the NF to increase as noise sources other than r_b begin to dominate. External impedance matching has lower loss

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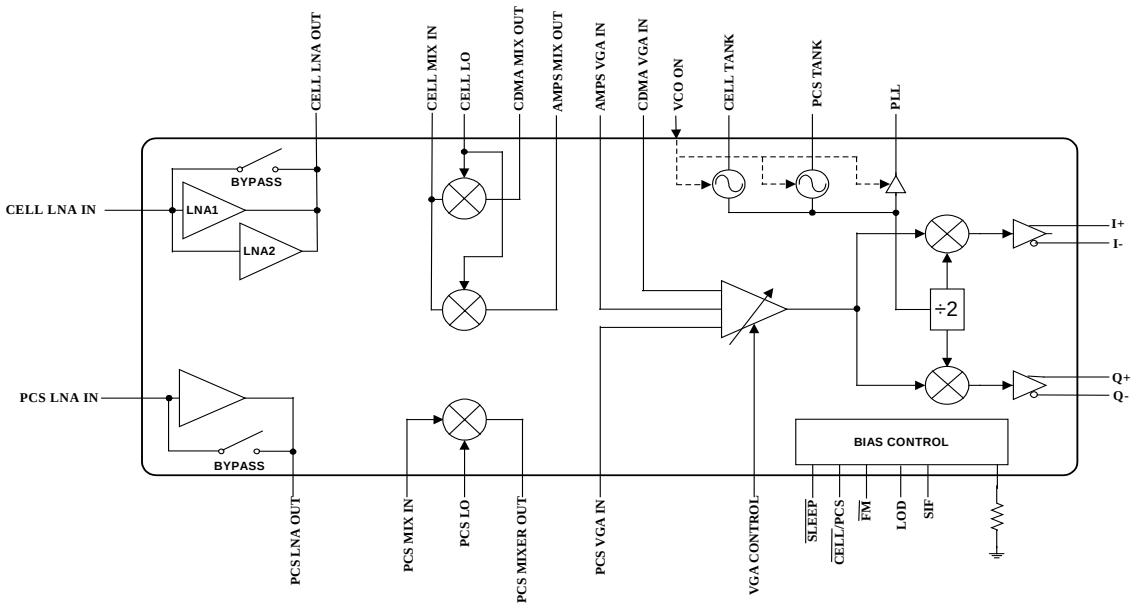

Fig. 1 Integrated receiver block diagram

than on-chip matching and allows optimization of the input match for all worldwide frequency allocations.

High IIP3 is achieved by feedback linearization from two sources. The first is inductive emitter degeneration (L_E) and the second is C_{CB} feedback. The emitter inductance is a bond wire and package pin to external ground. This provides the approximately 2 nH of inductance needed, with a higher Q than is possible with an on-chip inductor. The high Q means a low parasitic series resistance in the emitter and, correspondingly, a lower NF.

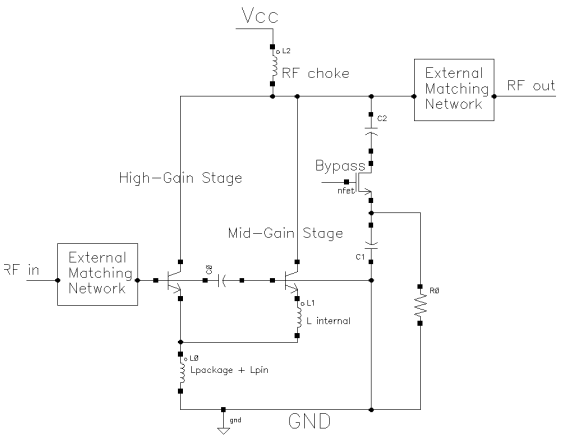

Fig. 2 Three step, switchable gain, cellular LNA

The current in the LNA device (I_C) is a key determinant of the IIP3, G and NF. A bipolar transistor's linearity improvement using emitter degeneration is roughly proportional to $I_C L_E$, the gain is proportional to $1/L_E$, and the NF is proportional to $1/\sqrt{I_C}$. Increasing I_C and reducing L_E gives improved linearity with higher G and lower NF, but results in high DC current. The device current must be optimized to balance the IIP3, G and NF.

The current used to bias the LNA is a bandgap bias that is derived from an external resistor. This ensures better absolute tolerance and less temperature variation than an on-chip resistor, as well as allowing the bias point to be varied externally according to the handset manufacturer's needs.

The mid-gain stage of the cellular LNA provides a lower gain with an even higher IIP3. This stage is also a common emitter configuration, with an additional on-chip inductor in series with the emitter to increase the linearity and reduce the gain. The needed increase in linearity can be arrived at by using less current and a larger, emitter inductance since the NF is not as important at this gain setting.

The mid-gain stage connects to the high gain stage through a low loss metal-insulator-metal (MIM) capacitor for DC blocking so that the two can be biased independently. This capacitor also helps to adjust the input match when the second stage is switched on, since the external match must work with all of the three gain steps.

For the bypass mode LNA devices are completely shut off and a MOSFET switch connects the input to the output. MIM capacitors are used for DC blocking and a large value resistor from the MOSFET's source to ground provides a ground reference for V_{GS}. The capacitors were optimized to preserve the input and

output matches, as well as minimize the bypass insertion loss. The cellular LNA's measured performance is given in Table I.

TABLE I
MEASURED PERFORMANCE OF CELLULAR LNA

	Gain [dB]	NF [dB]	IIP3 [dBm]	I_{DC} [mA]
High Gain Mode	16.3	1.6	5.6	8.0
Mid Gain Mode	7.6	2.5	12.0	5.0
Bypass Mode	-5.0	5.0	20.0	0.0
AMPS Mode	16.0	1.5	-1.0	4.5

The PCS LNA has a similar structure to the cellular LNA, but without the mid-gain stage. One difference from the cellular LNA is the use of downbonds to a package ground paddle for the emitter degeneration. The needed degeneration inductance is very small and three downbonds are used in parallel. The PCS LNA performance is given in Table II.

TABLE II
MEASURED PERFORMANCE OF PCS LNA

	Gain [dB]	NF [dB]	IIP3 [dBm]	I_{DC} [mA]
High Gain Mode	15.5	1.8	3.0	7.0
By Pass Mode	-4.0	4.0	21.0	0.0

B. RF Mixers

A standard Gilbert cell configuration was used for the RF mixers. In order to meet the high linearity requirements several techniques were used.

TABLE III
MEASURED PERFORMANCE OF RF MIXERS

	CDMA	AMPS	PCS
Gain [dB]	10.5	11.5	11.1
IIP3 [dBm]	8.5	6.1	6.1
NF [dB]	8.2	8.3	8.5
I_{DC} [mA]	18.0	12.0	18.0

Firstly, the input pair is inductively degenerated to provide the needed linearity with minimal loss of headroom. Since a reasonable amount of current is used to obtain the desired linearity, the resistive bias provided at the common mode point of the differential pair does not provide high enough impedance. Providing a parallel resonant tank at the common point of the input differential pair raises the bias impedance at RF. Finally, the high linearity requires a large output voltage swing, so external chokes to supply are used to bias the collectors.

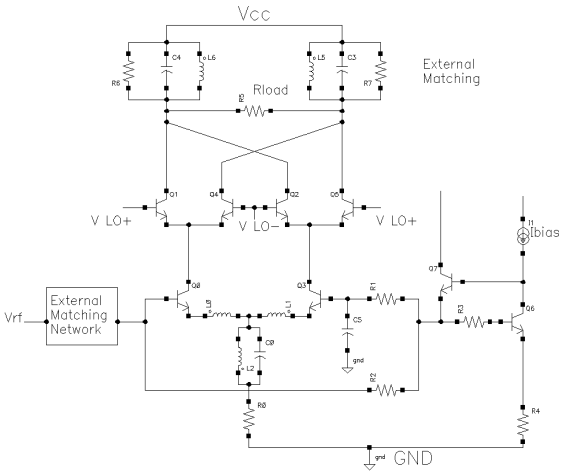

Fig. 3 Inductively degenerated Gilbert cell, with parallel resonant tank at the common mode bias point.

The CDMA and AMPS mixers share a common input and separate outputs (see Fig.1). The mixer that is off loads down the mixer that is active, therefore careful design of both mixers together must be done in order account for the loading. Also, the common input requires that a single, off-chip match be used for both modes adding additional constraints.

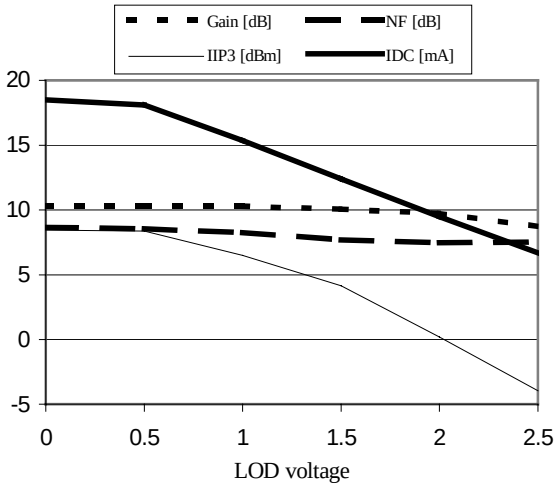

Fig. 4 CDMA mixer performance vs. LOD voltage

Flexibility is built into the design by separate bias control for the cellular and PCS mixer cores via external resistors. Linearity-On-Demand (LOD) is a feature built into the mixers. LOD allows a continuous, external control voltage to control the mixer IIP3 and reduce the mixer current from the nominal bias level. A large reduction in bias current has a minimal effect on the mixer gain. This feature can be used in strong wanted signal conditions and when blocker levels are low.

C. VGA/IQ Demodulators

The dynamic range needed by the receiver (in CDMA systems) is achieved by the VGA. The VGA has greater than 90dB of dynamic range, exceeding the 84dB of range of the TIA/EIA-98-C specification for CDMA [4]. The additional range allows for functionality despite variation resulting from the semiconductor processing, temperature effects, filter insertion losses, and external component variation.

At maximum gain, the VGA has minimum NF (<6dB) to reduce its contribution to the overall system NF. As gain reduces, the VGA maintains a NF less than 7.5dB for 15dB of control range so any variation in the maximum gain required does not cause a significant degradation in the achievable sensitivity. At the low end of the VGA gain range the IIP3 reaches a maximum greater than 7.5dBm in order to handle the large input signals. Analogous to the NF, the maximum IIP3 changes little for the first 20dB of control range as the gain begins to rise.

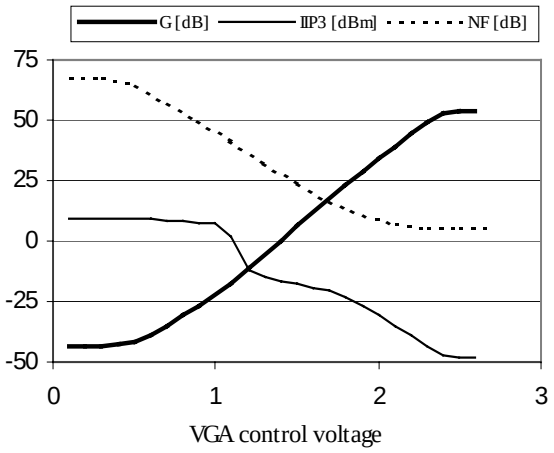

Fig. 5 VGA performance vs. control voltage

The VGA has inputs for each of the three modes of operation (CDMA, AMPS and PCS). The inputs for CDMA and PCS are differential to support commonly used IF SAW filters.

A pair of IQ demodulator mixers follows the VGA. The LO for these mixers is derived from a VCO with an on-chip active core and an external LC tank [4]. The VCO feeds to a divide-by-2 circuit to obtain a quadrature LO signal. Any DC offset present at the output of the IQ demodulator can cause the following analog baseband device to saturate due to the large amount of gain built up in the analog baseband. Thus, the IQ demodulator is designed to have a low output DC offset. Removing the DC offset with AC coupling capacitors is not desirable since the baseband AMPS signal occupies a narrow bandwidth. The coupling capacitor would be extremely large, causing a long startup time constant when the system is enabled.

Versatility is added to the receiver via an external logic control pin to enable a single-IF (SIF) to be used in CDMA and PCS modes. The motivation for this is to use a single IF SAW for both modes, saving cost and board area. To implement this the CDMA and PCS mixers' outputs are tied together externally and matched to the SAW. The SIF logic then enables a common VGA input and VCO. No change is made to the operation of the AMPS chain in the SIF mode.

IV. Conclusion

The integrated receiver presented supports multi-band, multi-mode cellular phones in some of the most demanding cellular systems, including WCDMA, CDMA, CDMA-PCS, and AMPS. While providing the block level performance to meet the specifications, additional features such as LOD are integrated to make the IC more attractive to phone manufacturers. The receiver enables smaller phone form factors and lower total cost.

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